IN THE CLAIMS

The following list of claims replaces all previous versions of the claims.

1. (Currently Amended) A method for communicating between a master device and a slave device connected via an inter-integrated circuit bus (I2C bus); said method comprising the steps of:

addressing said at least one slave device;

providing a command code to said addressed slave device, said command code comprising a plurality of bits, a first subset of said bits functioning as an indicator of a type of supplementary address that is being provided;

interpreting ~~a~~ said supplemental address contained in said command code; and,

determining an internal address for said slave device using said supplemental address.

2. (Original) The method of claim 1 wherein the slave device comprises at least one internal device having an internal address; and

wherein said interpreting step comprises using said supplemental address to determine at least part of said internal address.

3. (Original) The method of claim 1 wherein said communicating is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device.

4. (Cancelled)

5. (Currently Amended) The method of claim ~~4~~ 1 wherein a second subset of said plurality of bits comprises the supplemental address that is being provided.

6. (Original) The method of claim 2 wherein the command code comprises 8 bits and comprises a 2-bit indicator of a type of supplemental address that is being provided.

7. (Original) The method of claim 6 wherein a first state of said 2-bit indicator indicates that the supplemental address contains 6 bits of a 14-bit internal address that is being provided, said interpreting step comprising the steps of:

determining whether the 2-bit indicator is in said first state;

if said 2-bit indicator is in said first state, utilizing the 6 low order bits of the command code as part of the 14-bit internal address; and,

said determining step comprising the step of utilizing an additional 8 bits of data as the remainder of the 14-bit internal address.

8. (Original) The method of claim 6 wherein a second state of said 2-bit indicator indicates that the supplemental address contains 6 bits of a 6-bit internal address is being provided, said interpreting step comprising the steps of:

determining whether the 2-bit indicator is in said second state; and

if said 2-bit indicator is in said second state, utilizing the 6 low order bits of the command code as the 6-bit internal address.

9. (Original) The method of claim 8 wherein said communicating comprises a write operation being performed from said master device to said slave device, said method further comprising the steps of:

transitioning to a receive state responsive to receipt of said command code;

receiving data transmitted from said master device; and,

writing said data to the slave device at a location therein identified by said 6-bit internal address.

10. (Original) The method of claim 6 wherein a third state of said 2-bit indicator indicates that a direct write operation of data is being performed to a particular register on the slave device, said interpreting step further comprising:

responsive to said 2-bit indicator being in said third state, parsing the 6 low order bits of the command code to obtain said internal address which, when accessed, will cause the loading of predetermined data into said register via a hard-coded internal write operation.

11. (Original) The method of claim 6 wherein said 2-bit indicator indicates that one of two types
of supplemental addresses is being provided:

a 6-bit supplemental address that is used as part of a communicated 14-bit internal address; and,

a 6-bit supplemental address that is used as a 6-bit internal address.

12. (Original) The method of claim 6 wherein said 2-bit indicator indicates that one of two types of supplemental addresses is being provided:

a 6-bit supplemental address that is used as part of a communicated 14-bit internal address; and,

6-bit supplemental address that is used as a 6-bit internal address for a direct command access operation.

13. (Original) The method of claim 6 wherein said 2-bit indicator indicates that one of two types of supplemental addresses is being provided:

a 6-bit supplemental address that is used as a 6-bit internal address; and,

6-bit supplemental address that is used as a 6-bit internal address for a direct command access operation.

14. (Original) The method of claim 6 wherein said 2-bit indicator indicates that one of three types of supplemental addresses is being provided:

a 6-bit supplemental address that is used as part of a communicated 14-bit internal address;

a 6-bit supplemental address that is used as a 6-bit internal address; and,

6-bit supplemental address that is used as a 6-bit internal address for a direct command access operation.

15. (Original) A method for a master device to communicate with a slave device connected to said master device via an inter-integrated circuit bus (I2C bus); said method comprising the steps of:

generating an array of addressing parameters comprising an address of said slave device, an internal address within said slave device, and at least one indicator bit indicating the format of the internal address portion of the array; and,

transmitting said array over said I2C bus.

16. (Original) The method of claim 15 wherein said generating step comprises the step of:

generating a command code comprising said at least one indicator bit and at least a portion of said internal address.

17. The method of claim 15 wherein said generating step comprises the step of:

generating an array comprising an address of said slave device followed by a command code comprising said at least one indicator bit and at least a portion of said internal address followed by at least one array entry corresponding to said internal address.

18. (Original) The method of claim 17 wherein said communication is selected from the group consisting of writing data to a location within said slave device and reading data from a location within said slave device and wherein, when said communication is a writing, said method further comprising the step of transmitting data over said I2C bus.

19. (Original) The method of claim 17 wherein said generating step comprises the step of:

generating said array wherein said at least one indicator bit is in either a first state or a second state;

when said at least one indicator bit is in said first state, utilizing some of the command code as part of said internal address, and utilizing an additional portion of said array as the remainder of said internal address; and

when said at least one indicator bit is in said second state, utilizing some of the command code as all of said internal address.

20. (Original) The method of claim 19 wherein;

said command code comprises 8 bits;

the at least one indicator bit comprises the 2 high order bits of said command code;

when said 2 high order bits are in said first state, the 6 low order bits of said

command code comprise part of a 14-bit internal address, and an additional 8 bits of data in said array comprise the remainder of the 14-bit internal address; and

when said 2 high order bits are in said second state, the 6 low order bits of said command code comprise all of a 6-bit internal address.

21. (Original) The method of claim 20 wherein;

said 2 high order bits of said command code have a third state; and

when said 2 high order bits are in said third state, the 6 low order bits of said command code comprises an internal address associated with a particular register in said slave device that, when accessed, will cause the loading of predetermined data into said register via a hard-coded internal write operation.

22. (Original) A method for a slave device to communicate with a master device connected to said slave device via an inter-integrated circuit bus (I2C bus); said method comprising the steps of:

receiving an array of addressing parameters comprising an address of said slave device, an internal address within said slave device, and at least one indicator bit indicating the format of the internal address portion of the array;

interpreting said at least one indicator bit to determine the format of said internal address; and

interpreting said internal address portion of said array in accordance with said determined format.